IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of the claims in this application.

1. (Currently amended) A method for preventing passive release of interrupts within a computer system, the computer system having at least one processor for servicing the interrupts, one or more input/output (I/O) devices configured to issue interrupts, and an I/O bridge having a plurality of ports to which I/O devices are coupled and configured to interface between the I/O devices and the processor, the method comprising the steps of:

asserting an interrupt signal by a subject I/O device coupled to a given port of the I/O bridge;

forwarding an interrupt message corresponding to the interrupt signal to the processor for servicing;

setting an interrupt pending flag in response to assertion of the interrupt signal;

in response to the interrupt being serviced, generating a first ordered message, the first ordered message notifying the subject I/O device that the interrupt has been serviced;

generating a second ordered message for clearing the interrupt pending flag;

sending the first ordered message to the given port of the I/O bridge;

sending the second ordered message to the given port of the I/O bridge after the first message has been sent;

deasserting the interrupt signal in response to the first message; and

clearing the interrupt pending flag ~~at the interrupt file~~ in response to the second ordered message.

2. (Original) The method of claim 1 further comprising the step of forwarding the first ordered message from the given I/O bridge port to the subject I/O device.

3. (Original) The method of claim 2 wherein the step of deasserting the interrupt signal is performed by the subject I/O device following its receipt of the first ordered message.

4. (Currently amended) The method of claim 3 wherein one of the ports of the I/O bridge is ~~further includes~~ an interrupt port and the interrupt pending flag is disposed at the interrupt port, the method further comprising the step of forwarding the second ordered message from the given I/O bridge port to the interrupt port.

5. (Original) The method of claim 4 wherein

the interrupt pending flag is implemented through a register of the interrupt port; and

the second ordered message is a write transaction to the register for clearing the interrupt pending flag.

6. (Original) The method of claim 5 further comprising the steps of:

periodically collecting a set of information regarding the assertion of interrupt signals by I/O devices; and

after the step of clearing the interrupt pending flag, waiting a predetermined time before collecting a next set of information regarding the assertion of interrupt signals.

7. (Original) The method of claim 6 wherein the step of periodically collecting is performed through one or more serial data transfer operations.

8. (Original) The method of claim 1 wherein the steps of generating the first and second ordered messages are performed by the processor.

9. (Original) The method of claim 8 wherein the computer system includes (1) a plurality of processors at least one of which is designated to service interrupts from the subject I/O device, and (2) a plurality of I/O bridges each I/O bridge coupled to a plurality of I/O devices configured to assert respective interrupt signals.

10. (Not entered)

11. (Original) The method of claim 1 wherein the interrupt signals are level sensitive interrupts (LSIs).

12. (Currently amended) A computer system comprising:

a plurality of input/output (I/O) devices configured to assert and deassert respective interrupt signals;

at least one processor for servicing interrupts from the I/O devices; and

an I/O bridge configured to interface between the I/O devices and the at least one processor, the I/O bridge having a plurality of ports to which the I/O devices are coupled and an interrupt controller configured to detect the assertion and deassertion of the interrupt signals, wherein

the interrupt controller, in response to assertion of an interrupt signal by a subject I/O device coupled to a given ~~I/O bridge~~ port of the I/O bridge, issues an interrupt message to the at least one processor and sets an interrupt pending flag;

the at least one processor, upon servicing the interrupt, sends first and second ordered messages to the given port of the I/O bridge, the first ordered message notifying the subject I/O device that the interrupt has been serviced, and the second ordered message clearing the interrupt pending flag;

the subject I/O device deasserts the interrupt signal in response to the first message; and

the interrupt pending flag is cleared in response to the second ordered message.

13. (Currently amended) The computer system of claim 12 wherein

one of the ports of the I/O bridge is ~~further includes~~ an interrupt port at which the interrupt controller is disposed, and

the given port of the I/O bridge forwards the second ordered message to the interrupt port after forwarding the first ordered message to the subject I/O device.

14. (Original) The computer system of claim 13 wherein the interrupt port of the I/O bridge includes at least one register at which the interrupt pending flag is implemented.

15. (Original) The computer system of claim 12 wherein

the I/O bridge port includes a read cache for buffering messages received from the at least one processor, and an ordering engine operatively coupled to a read cache, and

the ordering engine is configured to release ordered messages buffered in the read cache in the same order as which they were received.

16. (Currently amended) The computer system of claim 12 further comprising an interrupt collector having a parallel-load shift register for receiving the interrupt signals from the I/O devices, the parallel-load ~~serial~~ shift register configured to transfer information indicating the assertion or deassertion of interrupt signals to the interrupt controller through one or more serial shift operations.

17. (Original) The computer system of claim 16 wherein

the interrupt collector transfers the information in response to a request from the interrupt controller, and

the interrupt controller is configured to limit the number of serial shift operations performed by the interrupt collector so as to receive only information associated with interrupt signals that have been enabled.

18. (Original) The computer system of claim 12 wherein the interrupt signals are level sensitive interrupts (LSIs).